

1. Fetch the instruction beginning at #500, and load load #12, A into the

instruction register. Increment the program counter to #502.

2. Decode load #12, A in the instruction register.

3. Execute load #12, A from the instruction register, using the memoryaccess

hardware.

4. Fetch the instruction beginning at #502, and load load #13, B in the

instruction register. Increment the program counter to #504.

5. Decode load #13, B in the instruction register.

6. Execute load #13, B from the instruction register, using the memoryaccess

hardware.

7. Fetch the instruction beginning at #504, and load add A, B, C into the

instruction register. Increment the program counter to #506.

8. Decode add A, B, C in the instruction register.

9. Execute add A, B, C from the instruction register, using the ALU and

register file.

10. Fetch the instruction at #506, and load store C, #14 in the instruction

register. Increment the program counter to #508.

11. Decode store C, #14 in the instruction register.

12. Execute store C, #14 from the instruction register, using the memoryaccess

hardware.

*revisit Chapter 1, and*

*particularly the sections“Refining the File-Clerk Model” on page 6 and “RAM: When*

*Registers Alone Won’t Cut It” on page 8.*